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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/587,465	06/05/2000	Jung-Cheng Lin	TSMC99-700	7855

28112 7590 04/15/2003

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EXAMINER
SARKAR, ASOK K

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/587,465	LIN, JUNG-CHENG	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/24/2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1 - 26 rejected under 35 U. S.C. 103(a) as being unpatentable for reasons of record in Paper No. 12 is reproduced below:

Claim Rejections – 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 10, 12 – 23, 25 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein, US 6,181,012 in view of Danek, US 5,943799 and Hsu, US 6,194,310, US 6,194,310.

Regarding claims 1 and 14, Edelstein teaches a method to prevent copper diffusion in an integrated circuit comprising:

- providing a substrate of wafer 52 (column 6, line 1) having an insulator layer 54 (column 6, line 62) deposited on the substrate 52 with reference to Fig. 2;
- providing first level of conducting wire 46 (column 6, line 64) over the insulator layer with reference to Fig. 2;
- depositing first and second dielectric layer 54 (column 6, line 62) over the first level of conducting wire 46 with reference to Fig. 2;
- patterning and etching the dielectric layers forming dual damascene trench/via openings 84 (column 7, line 40) with reference to Figs. 2 and 4A;

- depositing a barrier layer 72 (column 7, line 39) of W, WN and WSiN (column 9, line 31) covering and lining the trench with reference to Figs. 2 and 4A;
- depositing by electrochemical deposition (ECD) (column 7, line 57) a copper seed layer 76 or 86 (column 9, line 35);
- depositing by ECD copper conducting material 90 (column 7, line 42) over the seed layer (see column 7, lines 57 – 61) with reference to Figs. 2 and 4C and removing excess material layers to form the copper dual inlaid structure (see Figs. 2 and 4C) in column 7, lines 43 - 46;

Edelstein teaches barriers containing materials such as W, WN and WSiN but fails to teach depositing a first barrier layer of WN, then silanize the WN layer with reactive silane gas mixture to form WSiN over WN and depositing a W barrier layer to form a composite diffusion barrier layer structure of W / WSiN / WN.

Danek teaches a method of depositing composite multi-layer barrier structures especially comprising a layer sequence of W / WSiN / WN with reference to Figs 1 and 2 throughout the disclosure. Danek teaches the desirability of designing a suitable multi-layered diffusion layers in terms of integrity, resistivity and adhesion among other things in great detail. Danek teaches that TiSiN can be made by silane treatment of TiN and Hsu teaches that the same process can be applied for WSiN in column 5, lines 20 – 24.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure by incorporating a multi-layer barrier structure taught by Danek and Hsu by depositing a first barrier layer

of WN, then silanize the WN layer with silane gas to form WSiN over WN as taught by Danek and Hsu and depositing a W barrier layer to form a composite diffusion barrier layer structure of W / WSiN / WN so that a greatly improved barrier layer as taught by Danek is formed to prevent Cu diffusion.

Regarding claims 2 and 15, Edelstein teaches substrate 52 as an IC module with CMOS devices in column 6, lines 51 – 61.

Regarding claims 3 and 16, Edelstein teaches silicon dioxide dielectric/insulator in column 2, line 9.

Regarding claims 4 - 7 and 17 - 20, Edelstein does not teach the deposition process or the thickness of the layers of the composite barrier layer.

Danek teaches W and WN deposition by CVD and PECVD in column 5, lines 14 – 18 and barrier thickness less than 100 Angstroms in column 2, line31.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure to have the composite layered structure with appropriate thickness through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical

(*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237).

Regarding claims 8 and 21, Edelstein fails to teach the method of forming the WSiN layer.

Danek teaches the method for forming TiSiN by the silane treatment with ammonia at a temperature of 300°C in column 5, line 60 and column 6, line 14. As described earlier, Hsu teaches that processing of WSiN is similar to Ti.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure to have the composite layered structure containing WSiN layer on WN layer of appropriate thickness through routine experimentation and optimization to achieve optimum benefits.

Regarding claims 9 and 22, Edelstein teaches seed layer formation by ECD, PVD and thickness in column 9, lines 31 – 45.

Regarding claims 10 and 23, Edelstein teaches ECD process for forming the main copper conductor in column 7, lines 57 – 60.

Regarding claims 12 and 25, Edelstein teaches planarization to remove excess Cu by CMP in column 7, lines 44 – 46.

Regarding claims 13 and 26, Edelstein teaches multilevel interconnect structures for VLSI under the heading background of the invention.

Edelstein in view of Danek and Hsu does not teach creating multilevel structure by repeating the processes of claim 1 and 14.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's barrier layer structure to create multilevel structure by repeating the processes of claim 1 and 14 so that space saving multilevel IC structures can be made.

4. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein, US 6,181,012 in view of Danek, US 5,943799 and Hsu, US 6,194,310, US 6,194,310 as applied to claims 1 and 14 above, and further in view of Yu, US 6,291,332 and Hsu, US 6,054,382.

Edelstein in view of Danek and Hsu fails to teach ECD copper deposited on seed layer and barrier layer with fine grained <111> structure.

Yu teaches the relevance of <11> seed deposition which will ultimately result in fine grained Cu plug of <111> orientation in column 2, lines 28 – 40.

Hsu teaches the desirability of <111> texture of metal conductors for electromigration resistance in column 1, lines 21 – 26.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Edelstein's ECD Cu deposition in the trench so that fine grained Cu plug of <111> orientation is formed. <111> Cu texture results in the growth of fine-grained structure and fine-grained <111> textured Cu structure is more resistant to electromigration than the face-centered cube texture <100>.

Response to Arguments

5. Applicant's arguments filed March 24, 2003 have been fully considered but they are not persuasive.

6. Applicant's argues in page 4, 2nd paragraph that Danek and Hsu do not teach what barrier material or materials will yield good adhesion, barrier properties, enhance copper seed deposition and copper electroplating. Danek teaches many barrier materials including the materials claimed by the instant invention. The usefulness and the variety of materials available for multi-layer barrier purposes for copper interconnects are taught by Danek throughout their disclosure.

7. Regarding Applicant's argument in page 5, 1st paragraph that Danek fails to teach a three-component barrier layer, the Applicant is referred to his Fig. 4, where multiple stack of three component barrier is shown.

8. Regarding Applicant's argument in page 6, 1st paragraph about the silane soak, Danek teaches the same process for Ti and Hsu teaches the process for W. This process is a well-known prior art taught by Hsu and is routinely used by the industry for making conducting amorphous TiSiN and WSiN barrier layers in Cu damascene devices.

9. With regard to Applicant's argument for the seed layer deposition before copper electroplating, deposition of seed layer is a well-known prior art process. As was used in rejecting the claims, Yu does teach the need for <111> crystal orientation for the seed layer and therefore, a person with ordinary skill in the art will be motivated to use <111> crystal orientation for the seed layer in order to form a better adhering electroplated layer for the device.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 703 308 2521. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703 308 1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308 7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 4918.

Asok K. Sarkar
April 9, 2003